Design of a Bidirectional DC/DC Converter for Energy Storage in Electric Aircraft

Moanis Khedr
Department of Electronic & Electrical Engineering
University of Bath
Bath, United Kingdom
m.m.z.khedr@bath.ac.uk

Xianwu Zeng
Department of Mechanical Engineering
University of Bath
Bath, United Kingdom
xz2478@bath.ac.uk

Xiaoze Pei
Department of Electronic & Electrical Engineering
University of Bath
Bath, United Kingdom
x.pei@bath.ac.uk

***Abstract*— High-density power conversion and energy storage solutions were and are being explored for use in Electric Aircraft (EA). A superconducting magnetic energy storage (SMES) system is a promising candidate due to its fast response and ability to satisfy large pulse loads as is expected from EA. For the SMES, Dual Active Bridge (DAB) converters can offer high-density power conversion and provide galvanic isolation. This paper proposes a design methodology for a bidirectional DC/DC converter using DAB converter and a MOSFET-based chopper to interface SMES. This paper includes analysis, performance prediction, and needs for implementation in EA. The DAB/SMES system has been successfully designed, analyzed, and is being optimized for application in EA.**

Keywords— bidirectional, converter, dual active bridge, electric aircraft, energy storage, superconducting

I. INTRODUCTION

With the rise in research into More Electric Aircraft (MEA), there is more need for high-density power conversion and energy storage solutions, increasing research into improving existing solutions (e.g., new control schemes) and different operation modes (e.g., cryogenic operation of power switches) [1]-[7].

For power conversion, a potential solution that assumes the use of a DC microgrid (like Turboelectric Aircraft) is a Dual Active Bridge (DAB) converter which provides bidirectional power flow for charging/discharging energy storage systems, galvanic isolation to minimize system noise, be able to connect/disconnect storage systems and allow different input/output voltages. The design flexibility of integrating more bridges or changing control schemes, not to mention the inherent Zero-Voltage-Switching (ZVS) to an extent (mostly at high converter loading) are additional benefits of DAB converters [1]-[6].

As for energy storage systems (ESSs), one option is to use a Superconducting Magnetic Energy Storage (SMES) system, as they have much higher power density than batteries, supercapacitors, etc., faster response times in milliseconds, very long operational lifetimes, high cycle life, and can satisfy large pulse loads, though its disadvantages include higher cost per kW, relatively high parasitic losses (mostly from using power switches for the chopper circuit), and the obvious need for constant cryogenic cooling [9]-[11].

While current literature has separately explored using DAB converters for different loads [3]-[6] and some ESSs [8], and SMES integration into systems (terrestrial grids via chopper or hybrid solution for EA) [9]-[11], none have tried to combine both for EA. This paper proposes a methodology to design and control a combined DAB/SMES system for use in EA, presents its operation using the PLECS simulation platform, discusses its implementation, and uses simulations to predict its performance.

II. OVERVIEW OF THE DUAL ACTIVE BRIDGE CONVERTER WITH SMES

The chosen specifications are shown in Table 1. They are tentative to represent use in an on-board DC microgrid, but the design process remains the same and only minor changes would be needed to the process in some cases (a calculation for sizing filter capacitors and ZVS limit analysis). The Single Phase-Shift (SPS) DAB and the chopper to interface with the SMES are used to have a baseline to improve upon and as they have both been widely covered in literature. MOSFETs are used in the chopper circuit instead of IGBTs and Diodes to reduce the standby loss [12]. Fig. 2 shows the combined DAB/SMES circuit, and the current flow during one of the two main conduction half-cycles of the DAB during operation. Note that the switch names (i.e., S1, etc.) refer to the whole unit, i.e., the MOSFET with the antiparallel diode.

TABLE I. KEY SPECIFICATIONS

Converter Specifications		**SMES Specifications**	
Switching Frequency	100 kHz	***SMES Inductance***	862 mH
Bus Voltage (from MEA literature)	270 V	***Maximum Current/Power***	373.3 A / 100.8 kW
SMES-side Voltage	270V	***Maximum Stored Energy***	60 kJ
Transformer Turns Ratio	1:1	***Charging Time (at 270 V)***	1.2 s
Maximum/Rated Power	105 kW / 100.8 kW	**SMES Under Load**	
Voltage Ripple target at P_{rated}	0.6% / 1.6 V	***Example Load***	50 kW / 185.2 A
Leakage Inductance (Result)	0.87 µH	***Discharge time at full load***	0.9 s
Filter Capacitors (Result)	500 µF	***Energy Discharged/ Remaining***	45.2 kJ / 14.8 kJ

III. SIZING THE DUAL ACTIVE BRIDGE

The SPS DAB converter is a well-known topology with many variations presented in literature. The first step in designing it is to size its leakage inductance, which is usually sized at the maximum desired power, P_{max}, which occurs at 50% phase shift, as determined using (1), (2) and (3):

$$P_{out}=\frac{nx\times V_{hv}\times V_{lv}\times d(1-d)}{2f_s\times L_{ext}} \tag{1}$$

$$P_{out}=\frac{nx\times V_{hv}\times V_{lv}\times d(1-d)}{2f_s\times L_{ext}}\xrightarrow[P_{max}]{d=0.5} L_{ext}=\frac{nx\times V_{hv}\times V_{lv}}{8\times f_s\times P_{max}} \tag{2}$$

$$d=t_{delay}\times 2f_s \leftrightarrow t_{delay}=\frac{d\times T_s}{2} \tag{3}$$

Where L_{ext} is the inductance, f_s and T_s are the switching frequency and period ($T_s=1/f_s$), nx (or n) is the turns ratio, V_{hv} and V_{lv} are the Bus-side and SMES-side voltages (high and low voltages usually), d is the phase shift between the primary

978-0-7381-1301-2/21/$31.00 ©2021 IEEE

and secondary bridges, and P_{out} and P_{max} are the expected output/load and maximum powers, respectively. These are the main design parameters of a SPS DAB DC-DC converter.

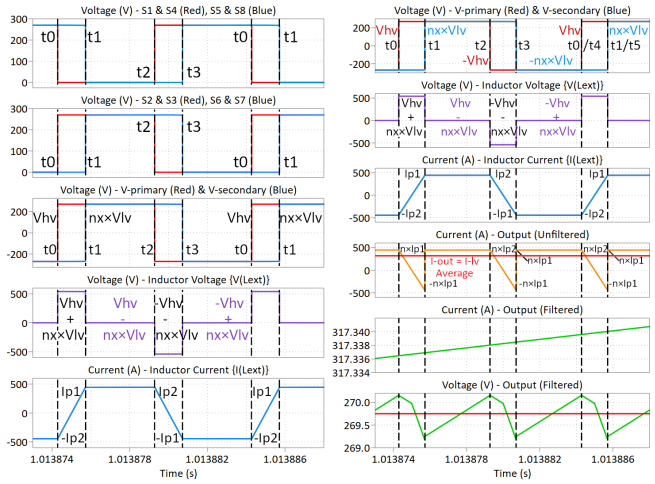


Fig. 1. Key DAB waveforms during charging mode

Now that the leakage inductance of the DAB has been sized appropriately, the filter capacitors need to be sized to minimize ripples, which can be critical for a SMES as high-frequency ripples in superconductors can result in additional AC losses. Before that however, the peak inductor currents and average output current in both charging and discharging modes need to be calculated at maximum power (i.e., P_{max} at d=0.5). The equations used to determine them are as follows:

$$I_{p1}=\frac{V_{hv}\times(2d-1)+(nx\times V_{lv})}{4\times f_s\times L_{ext}} \tag{4}$$

$$I_{p2}=\frac{nx\times V_{lv}\times(2d-1)+V_{hv}}{4\times f_s\times L_{ext}} \tag{5}$$

$$I_{lv}=\frac{P_{out}}{V_{lv}}=\frac{nx\times V_{hv}\times d\times(1-d)}{2\times f_s\times L_{ext}} \tag{6}$$

$$I_{hv}=\frac{P_{out}}{V_{hv}}=\frac{nx\times V_{lv}\times d\times(1-d)}{2\times f_s\times L_{ext}} \tag{7}$$

Where I_{p1} and I_{p2} are the two peak inductor currents, as seen in Fig. 1 with the main switching intervals of the two bridges, I_{lv} is the average SMES-side output current at a given P_{out} during charging mode, and I_{hv} is the average Bus-side output current at a given P_{out} during discharging mode.

The inductor current peaks are derived using the inductor voltages and currents observed in Fig. 1 and the standard inductor voltage-current-time relationship described in (8). From the current peaks, the average inductor and output currents can be derived with derivations discussed in [8], briefly discussed in [5] and [6] and verified in their citations.

$$V=L\frac{di}{dt}\leftrightarrow\int di=\frac{\int V\cdot dt}{L} \tag{8}$$

For the charging mode, the SMES-side filter capacitor would need to be sized. To do so, the time periods during which the unfiltered SMES-side output current (orange in Fig. 1) is above the average current (red) are calculated, which are $t_{\Delta1}$ (time between $nx\times I_{p1}$ and $nx\times I_{p2}$, or t_1 and t_2) and $t_{\Delta2}$ (between $nx\times I_{p2}$ and I_{lv}), after which the charge during these intervals can be determined ($Q_{\Delta1}$ and $Q_{\Delta2}$, respectively). The capacitor C_{lv} can be sized using the percentage of ripple required at the rated power (0.6% at 100.8 kW). From Fig. 1, the behavior described by (8), the time periods, charges, and ripple during charging are determined by (9)-(13), where $Q_{\Delta1}$ and $Q_{\Delta2}$ are the charges during $t_{\Delta1}$ and $t_{\Delta2}$, r_{lv} is the SMES-side voltage ripple, and C_{lv} is the SMES-side filter capacitor.

$$t_{\Delta1}=t_2-t_1=\frac{1-d}{2\times f_s} \tag{9}$$

$$t_{\Delta2}=\frac{(I_{p2}-(I_{lv}/nx))\times L_{ext}}{V_{hv}+(nx\times V_{lv})} \tag{10}$$

$$Q_{\Delta1}=\frac{1}{2}\times\Big((nx\times I_{p1}-I_{lv})+(nx\times I_{p2}-I_{lv})\Big)\times t_{\Delta1} \tag{11}$$

$$Q_{\Delta2}=\frac{1}{2}\times(nx\times I_{p2}-I_{lv})\times t_{\Delta2} \tag{12}$$

$$r_{lv}=\frac{\Delta v_{lv}}{V_{lv}}=\frac{\Delta Q_{lv}}{C_{lv}\times V_{lv}}\leftrightarrow C_{lv}=\frac{Q_{\Delta1}+Q_{\Delta2}}{r_{lv}\times V_{lv}} \tag{13}$$

A similar method of determining voltage ripple is shown in [5] and [6], however an alternate method is used to determine $t_{\Delta1}$ here, since the value of the denominator (i.e., V_{hv}-$nx\times V_{lv}$) would have been zero in this case, though both methods provide the same result (i.e., the time during which both primary and secondary bridge voltages are in phase).

Similarly, the Bus-side filter capacitor can also be sized, with $nx\times I_{p1}$, $nx\times I_{p2}$ and I_{lv} replaced by I_{p1}, I_{p2} and I_{hv}, to determine the time periods, charges, and ripple as follows:

$$t_{\Delta2}=\frac{(I_{p1}-I_{hv})\times L_{ext}}{V_{hv}+(nx\times V_{lv})} \tag{14}$$

$$Q_{\Delta1}=\frac{1}{2}\times\Big((I_{p2}-I_{hv})+(I_{p1}-I_{hv})\Big)\times t_{\Delta1} \tag{15}$$

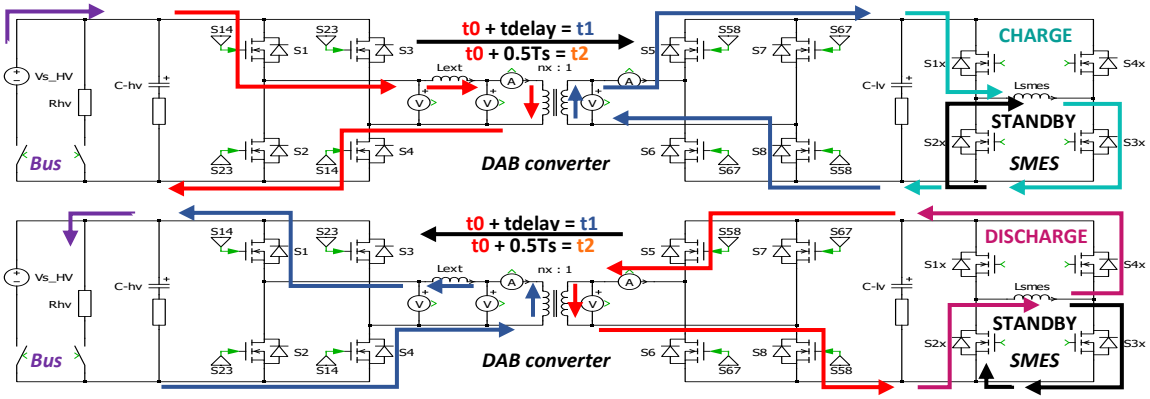


Fig. 2. Combined DAB/SMES circuit diagrams with current flow during charging mode (top) and discharging mode (bottom)

$$Q_{\Delta 2}=\frac{1}{2}\times\left(I_{p1}-I_{hv}\right)\times t_{\Delta 2} \tag{16}$$

$$r_{hv}=\frac{\Delta v_{hv}}{V_{hv}}=\frac{\Delta Q_{hv}}{C_{hv}\times V_{hv}}\leftrightarrow C_{hv}=\frac{Q_{\Delta 1}+Q_{\Delta 2}}{r_{hv}\times V_{hv}} \tag{17}$$

Where $Q_{\Delta 1}$, $Q_{\Delta 2}$, and $t_{\Delta 2}$ here are the equivalents of the previous terms on the Bus-side bridge output, r_{hv} is the Bus-side voltage ripple, and C_{hv} is the Bus-side filter capacitor. Note that determining $t_{\Delta 1}$ using (9) is valid for both modes.

While the converter was sized at 105 kW at 50% phase shift (d=0.5), the rated power is 100.8 kW at 40% shift (d=0.4) to lower RMS current and current peaks, and those are used in the previous equations to determine parameters, with the average current reaching 373.3 A, while the current peaks reach 625.4 A at 100.8 kW and 40% shift. If a specific output power is preferred for sizing, or to determine the currents at that output, the value of the phase shift, d, can be determined by converting (1) into a quadratic equation as shown in (18), solving it, and using the lower value of d in the previous equations. The effect of phase shift on RMS currents is noted among the design challenges in Section VI.

$$d^2-d+\left(\frac{P_{out}\times 2f_s\times L_{ext}}{nx\times V_{hv}\times V_{lv}}\right)=0 \tag{18}$$

Also, as noted from simulations, if the output voltage drops, and the PI controller becomes slightly unstable whether from imperfect tuning or other reasons while the DAB is operating at or near 50% phase shift, it may overcompensate and increase the phase shift beyond 50%, leading to a significant increase in RMS currents, inductor current peaks, and thus losses, despite resulting in the same average currents.

IV. Sizing the Superconducting Magnetic Energy Storage System

The SMES must also be sized for this system, and as such needs a target load and the time for which it must be maintained, since that determines the energy that needs to be supplied, and that along with the peak converter current may be used to size the inductance of the SMES. With that in mind, the required inductance for the SMES is determined by:

$$T_{disc}=\frac{Esmes_{max}-Esmes_{min}}{P_{load}}=\frac{L_{smes}}{2}\times\frac{I_{max}^2-I_{lv}^2}{V_{lv}\times I_{lv}} \tag{19}$$

$$T_{disc}=\frac{L_{smes}}{2}\times\frac{I_{max}^2-I_{lv}^2}{V_{lv}\times I_{lv}}\rightarrow L_{smes}=\frac{2\times P_{load}\times T_{disc}}{I_{max}^2-I_{lv}^2} \tag{20}$$

Where L_{smes} in the SMES inductance, P_{load} is the bus-side load to be fed, T_{disc} is the discharge time, E_{smes} refers to the SMES stored energies (at max. and min. load maintaining currents), I_{max} refers to the maximum SMES current (i.e., peak rated SMES-side current for the DAB converter), and I_{lv} here is the SMES-side current under the considered bus-side load ($I_{lv}=P_{load}/V_{lv}$). Additionally, the maximum and minimum SMES energies can be determined as noted in (19) and (20), while the SMES' charging time (T_{charge}) can be calculated by:

$$T_{charge}=\frac{L_{smes}\times I_{max}}{V_{lv}} \tag{21}$$

For the example noted in Table I, a 50 kW Bus-side load at 13.9% shift (d=0.139) is assumed to be fed for 0.9 s (i.e., 45.2 kJ discharged). Using the load and peak SMES currents, 185.2 A and 373.3 A, respectively, in (20) results in a required SMES inductance of 862 mH. From the example and (20), if the desired load is higher, either the discharge time is reduced for the same inductance (e.g., 85 kW for 0.2 s using 862 mH), or the inductance is increased to have more energy available. Thus, the SMES' energy levels depend on the separation between the SMES' peak current and the load current, and the SMES' design depends on optimising the desired load power/current and the charging/discharge times.

V. Control of the Dual Active Bridge and the SMES

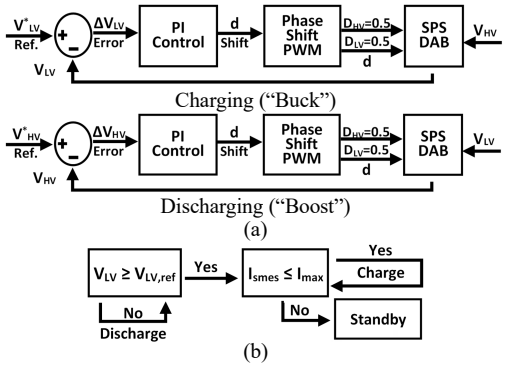


Fig. 3. Simplified control block diagrams for: (a) SPS DAB and (b) SMES

Now that the two sections have been sized and designed, they need to be combined. To do so, their operational schemes must be discussed, since a traditional SMES uses a chopper as previously stated, and that system would attach directly to the bus in its simplest form. Simplified control block diagrams for the charging mode are as seen in Fig. 3, with the charging and discharging control loops for the DAB shown in Fig. 3(a) and the SMES control loop in Fig. 3(b). As can be seen, the two loops work in tandem but are not combined as the SMES chopper is still used here.

As seen in Fig. 3(a), for the SPS DAB charging scheme, the difference between actual and reference voltages are given to a PI controller to get the phase shift between the primary and secondary bridges that is needed to achieve the reference voltage. The parameter that is controlled via the phase shift is the SMES-side voltage during the charging mode, with the phase shift being positive, while the Bus-side voltage is controlled during the discharging mode, with the phase shift being negative. Additionally, a fixed 50% duty cycle is used across all switches (since this is the traditional Single Phase-Shift scheme), resulting in the waveforms seen in Fig. 7.

As for the SMES control scheme in Fig. 3(b), its operation is straightforward, charging whenever the SMES-side voltage is at or above the reference voltage until the inductor current reaches its peak rating (373.3 A), while it discharges when the current SMES-side voltage is under the reference voltage. This means that the SMES recharges the SMES-side capacitor whenever its voltage drops, and they both act concurrently as the power source for the DAB during the discharging mode.

In terms of simulation, as in the circuit diagram in Fig. 2, where operation is forced in one direction or the other, and only a DC voltage source and a resistive load are used on the Bus-side, these loops seem to provide satisfactory operation as will be shown in Section VII. The main change for a larger simulation study, which would involve an EA microgrid on the Bus-side instead of a voltage source/resistive load setup, would include a timed delay for the charging mode to avoid

charging during or soon after a major or complete loss of system power supply.

When implemented within a complete electric aircraft system, additional parameters and conditions need to be considered for control. For example, if the bus operates at a wide range of voltages, peak, nominal, and minimum bus voltages need to be considered for both sizing and control. Another case is for power levels and thus different bus current levels, meaning there would be a minimum bus current to allow charging, and a minimum bus current under which discharging would occur, with voltages considered similarly.

For physical implementation, as MOSFETs are used across the DAB/SMES system to minimize losses, dead times must be implemented to avoid short-circuits on the same leg. In the SMES chopper specifically, dead times introduce intermediate charging and discharging states where the diodes conduct momentarily. Finally, both control loops are operated at 100 kHz in the simulation but may be lowered for actual implementation to allow for sampling and computational delays [12]-[13]. In PLECS, the system's control loops were operated at 50 and 25 kHz with no major changes.

VI. Challenges in Designing a DAB/SMES System

The main DAB design parameters are voltages, power, and frequency, and in terms of operation, there are three main design challenges: Zero Voltage Switching (ZVS), switch losses, and transformer design. This section discusses the impact and process behind selecting the parameters prior to finalizing the system design to deal with those challenges.

A. Zero Voltage Switching (ZVS)

The soft-switching operational range of the DAB is limited by the operational duty cycle, the Bus and SMES-side voltages (V_{hv} and V_{lv}, respectively), and the transformer's turns ratio (nx). The specifics are discussed below using the voltage ratio, M, described in (22).

$$M=\frac{nx\times V_{lv}}{V_{hv}} \tag{22}$$

As seen in Fig. 1, each major switching operation during the charging mode coincides with one of the two current peaks. To look at the conditions behind this, Fig. 4 is used to show the Bus and SMES-side switch voltages and currents as well as the inductor current during a charging mode half-cycle. The ZVS conditions and analysis are the same for the discharging mode and are thus not duplicated here.

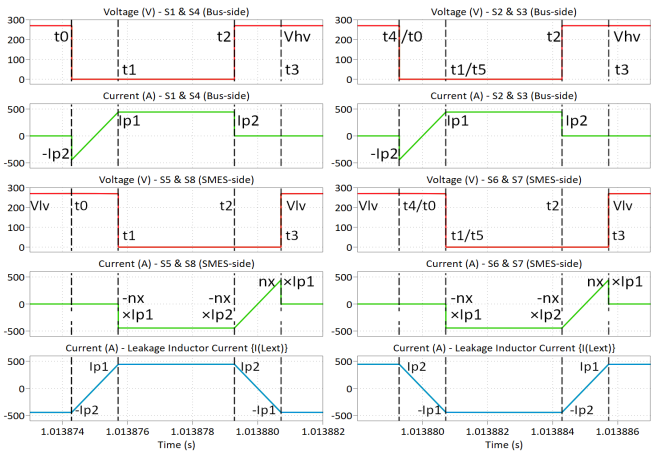


Fig. 4. Bus-side and SMES-side switches with leakage inductor current

From Fig. 4, it can be noted that the Bus-side MOSFETs initially reverse conduct before forward conducting for most of the conduction time, while the SMES-side MOSFETs reverse conduct for the most part before forward conducting at the end, allowing for ZVS operation in both bridges.

As seen in Fig. 4, $-I_{p2}$ is the current the Bus-side switches experience at turn-on at t_0, and as I_{p2} itself is positive, the current through the Bus-side switches initially flows in the MOSFET's reverse direction before reversing direction and flowing forward through the MOSFET. This means that for Bus-side switches to have ZVS to minimize losses, I_{p2} must be greater than zero (i.e., positive). Taking I_{p2} from (5), dividing both the numerator and denominator by the Bus voltage V_{hv}, and using the voltage ratio in (22) result in (23) and (24), which define the Bus-side ZVS range in terms of the phase shift and voltage ratio of the DAB converter.

$$I_{p2}=\frac{(nx\times V_{lv}\times(2d\text{-}1)+V_{hv})/V_{hv}}{4\times f_s\times L_{ext}/V_{hv}}\geq 0\rightarrow M\times(2d\text{-}1)+1\geq 0 \tag{23}$$

$$d\geq\frac{M\text{-}1}{2\times M} \tag{24}$$

Similarly, as can be seen in Fig. 4, $-nx\times I_{p1}$ is the current the SMES-side switches experience at turn-on at t_1, and as I_{p1} itself is positive, the current through the SMES-side switches flows in the MOSFET's reverse direction for most of the conduction period before reversing direction and flowing forward through the MOSFET. This means that for SMES-side switches to have ZVS to minimize losses, I_{p1} must be greater than zero (i.e., positive). Taking I_{p1} from (4), dividing both the numerator and denominator by the Bus voltage V_{hv}, and using the voltage ratio in (22) result in (25) and (26), which define the SMES-side ZVS range in terms of the phase shift and voltage ratio of the DAB converter.

$$I_{p1}=\frac{(V_{hv}\times(2d\text{-}1)+(nx\times V_{lv}))/V_{hv}}{4\times f_s\times L_{ext}/V_{hv}}\geq 0\rightarrow(2d\text{-}1)+M\geq 0 \tag{25}$$

$$d\geq\frac{1\text{-}M}{2} \tag{26}$$

Based on (24) and (26), a graph showing the range of ideal ZVS operation can be plotted against the voltage ratio (M) and operational phase shift (d) as seen in Fig. 5, with areas where ZVS is retained or lost denoted for a SPS DAB converter.

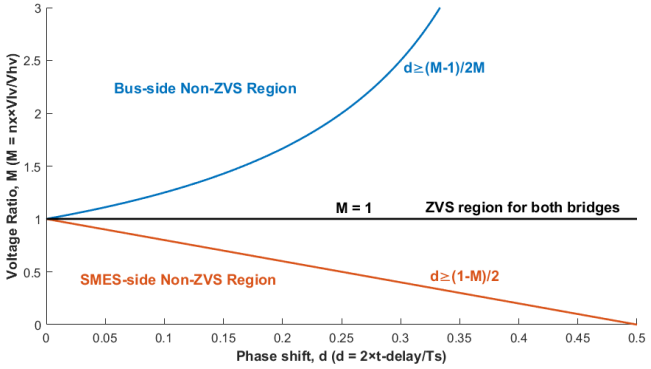


Fig. 5. ZVS and non-ZVS operational ranges for a SPS DAB converter

B. RMS currents

For the switch losses and transformer design, they both involve the RMS inductor current and inductor current peaks since they determine the currents and losses across the

transformer and the switches, in addition to transformer core and winding designs, cooling, etc. From the current peaks in (4) and (5) and from the waveforms in Fig. 1, the RMS inductor current can be derived, with the full derivations discussed in [8]. The main equations used to determine the RMS inductor current during the charging mode are thus:

$$t_{B1}=\frac{V_{hv}+(nx\times V_{lv}\times(2d-1))}{4\times f_s\times(V_{hv}+nx\times V_{lv})} \tag{27}$$

$$I_{\Delta p}=I_{p2}-I_{p1} \tag{28}$$

$$A_1=\frac{1}{3}\times I_{p1}^2\times\left(t_{delay}-t_{B1}\right) \tag{29}$$

$$B_1=\left(\frac{T_s}{2}-t_{delay}\right)\times\left(I_{p1}^2+\frac{I_{\Delta p}^2}{3}+I_{\Delta p}\times I_{p1}\right) \tag{30}$$

$$C_1=\frac{1}{3}\times I_{p2}^2\times t_{B1} \tag{31}$$

$$I_{rms1}=\sqrt{\frac{2}{T_s}\times(A_1+B_1+C_1)} \tag{32}$$

Where I_{rms1} is the RMS inductor current during the charging mode, t_{B1} is the time between I_{p2} and the inductor current reaching zero, t_{delay} is the phase shift between the primary and secondary bridges in seconds as seen in (3), f_s and T_s are the switching frequency and period ($T_s=1/f_s$), $I_{\Delta p}$ is the difference between the two inductor current peaks, and A_1, B_1, and C_1 are parts of (32) separated for clarity. In a similar manner, the RMS inductor current during the discharging mode can be determined as follows:

$$t_{B2}=\frac{(nx\times V_{lv})+V_{hv}\times(2d-1)}{4\times f_s\times(V_{hv}+nx\times V_{lv})} \tag{33}$$

$$A_2=\frac{1}{3}\times I_{p2}^2\times\left(t_{delay}-t_{B2}\right) \tag{34}$$

$$B_2=\left(\frac{T_s}{2}-t_{delay}\right)\times\left(I_{p2}^2+\frac{I_{\Delta p}^2}{3}-I_{\Delta p}\times I_{p2}\right) \tag{35}$$

$$C_2=\frac{1}{3}\times I_{p1}^2\times t_{B2} \tag{36}$$

$$I_{rms2}=\sqrt{\frac{2}{T_s}\times(A_2+B_2+C_2)} \tag{37}$$

Where I_{rms2} is the RMS inductor current during the discharging mode, t_{B2} is the time between I_{p1} and the inductor current reaching zero, t_{delay} is the phase shift between the primary and secondary bridges in seconds as noted in (3), f_s and T_s are the switching frequency and period ($T_s=1/f_s$), and A_2, B_2, and C_2 are parts of (37) separated for clarity. Given the same input parameters, (32) and (37) will give the same result.

Now that the RMS currents can be determined along with the current peaks, I_{p1} and I_{p2}, they can all be used to determine whether a chosen design meets loss and efficiency targets, feasibility in terms of current and voltage stress for device selection (equations covering per device stresses are derived and shown in [8]), design targets for the transformer, etc.

In the scenario described in the overview in Section II, the system shown here had pre-determined voltages, transformer turns ratio, and peak power requirements, thus narrowing down DAB design. However, if a specific operating load and Bus voltage were targeted, and the system was to be built around optimal RMS current, a different approach is used.

For example, assuming the DC bus voltage is 270 V, and a nominal load of 50 kW, Equation (1) can be rearranged to calculate the leakage inductance L_{ext}. Then using (4), (5), (22), and (27)-(32) to determine the inductor current peaks and RMS values under various voltage ratios and target phase shifts, the range of RMS currents can be determined and plotted as seen in Fig. 6.

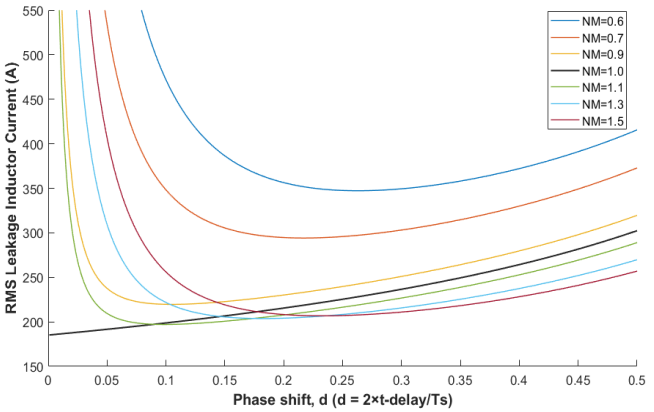
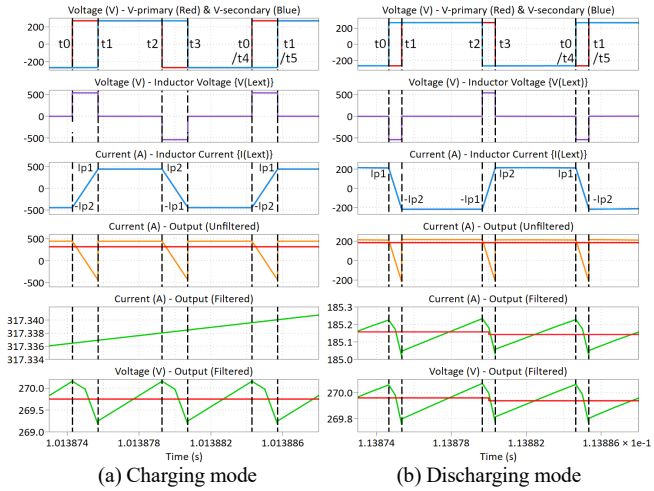


Fig. 6. RMS current vs duty cycle at different voltage ratios

As can be seen in Fig. 6, the design used in this paper, with a voltage ratio of 1 (i.e., M=1) and targeting 50 kW at a 13.9% phase shift (d=0.139) results in nearly the lowest RMS current at 204.8 A. In this case, lower voltage ratios (i.e., $V_{hv} > nx\times V_{lv}$) always resulted in higher RMS inductor currents, while higher voltage ratios (i.e., $V_{hv} < nx\times V_{lv}$) resulted in lower RMS currents at higher phase shifts. Similar plots can also be made for the current peaks. Additionally, the design can be varied provided the leakage inductance and transformer design are physically and electrically feasible and provided the SMES-side voltage is not fixed or limited by other factors.

VII. Simulated System Operation and Results



(a) Charging mode (b) Discharging mode

Fig. 7. Key DAB waveforms during charging and discharging modes

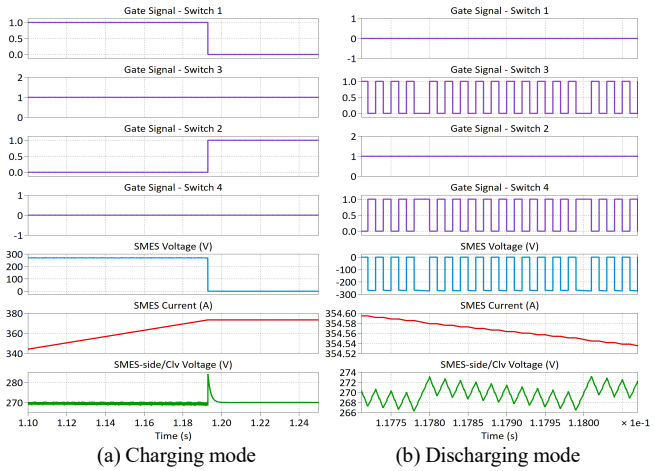
As the DAB and SMES have been sized and the control schemes have been implemented, the performance, and the operational waveforms of the DAB/SMES system need to be shown to explain and observe its operation, and to determine how and where improvements can be made. As the circuit diagram and waveforms are shown and DAB operation can be

derived in the same way in both modes, only the DAB section's charging mode operation will be detailed in this section. Fig. 7 shows some key current and voltage waveforms concerning the performance of the DAB section of the system.

Using Fig. 7 as well as the circuit diagrams in Fig. 2 for reference, the DAB charging operation can be explained. Practical dead-times aside, there are five main switching times in a switching cycle (T_s): t_0 at which the first Bus-side switch set, S1 and S4, are turned on; t_1 when the complementing SMES-side switches, S5 and S8, are turned on; t_2 when S3 and S2 are turned on after turning off S1 and S4; t_3 when S6 and S7 are turned on after turning off S5 and S8; and finally the next t_0 (also called t_4) when S1 and S4 are turned on again. These details can be seen more clearly in Fig. 4.

During the main conduction periods when both the primary and secondary voltages are in phase, i.e., between t_1 and t_2, and between t_3 and t_4/t_0, only forward conduction occurs through the Bus-side MOSFETs while only reverse conduction occurs through the SMES-side MOSFETs. During the intermediate periods when the primary and secondary voltages are not in phase, i.e., between t_0 and t_1 or between t_2 and t_3, current shifts direction in both bridges prior to the next conduction period, leading to a "power backflow" (called reactive power in some studies) where no useful power is delivered to the load. This facilitates the soft switching inherent to the DAB, but also causes higher RMS current and current peaks. These limits, explained in Section VI, have been described and mitigated in literature, and solutions will be explored in this system in future works [1]-[6] [8] [13] [14].

Fig. 8 shows the gate signals of the SMES chopper (1 is On, 0 is Off), the voltage and current of the SMES, and the SMES-side capacitor voltage, during both modes. Based on the control scheme in Fig. 3(b), switches S1x and S3x are turned on to charge the SMES until it reaches its peak current, at which point S1x and S2x are turned off and on, respectively, to enable the standby mode of the SMES chopper. When the SMES switches to standby mode, as seen in Fig. 8 (a), the SMES-side voltage spikes since the DAB still delivers power and the load is now just the filter capacitor. The frequency and tuning of the PI controller will affect the duration and peak of the voltage spike, but it should minimize the duty cycle to near zero as it will now simply maintain the capacitor voltage at the reference voltage until the SMES current decreases.



(a) Charging mode (b) Discharging mode

Fig. 8. SMES waveforms and SMES-side capacitor voltage in both modes

During the discharging mode, the SMES chopper alternates between its standby and discharging modes, the latter of which sees S2x and S4x turned on to discharge the SMES and thus maintain the SMES-side voltage at or above the reference voltage, then switching to standby at times when that condition is fulfilled, as seen in Fig. 8 (b). The current flow for the SMES in all modes is also shown in Fig. 2.

VIII. Conclusions

This paper focused on the design methodology combining a DAB converter and full bridge chopper for SMES integration to provide a high-power density solution for EA. The system was successfully designed with component sizing and control schemes discussed for both the charging and discharging modes, in addition to briefly discussing the challenges involved in physically implementing the system. Soft-switching requirements and reduction of RMS currents, current peaks, and thus losses, were also considered during the design process. And finally, the performance of the combined system was presented using the PLECS simulation platform.

References

[1] A. Barzkar and M. Ghassemi, "Electric Power Systems in More and All Electric Aircraft: A Review," in *IEEE Access*, vol. 8, pp. 169314-169332, 2020.

[2] L. Dorn-Gomba, J. Ramoul, J. Reimers and A. Emadi, "Power Electronic Converters in Electric Aircraft: Current Status, Challenges, and Emerging Technologies," in *IEEE Transactions on Transportation Electrification*, vol. 6, no. 4, pp. 1648-1664, Dec. 2020.

[3] Q. Xu, N. Vafamand, L. Chen, T. Dragičević, L. Xie and F. Blaabjerg, "Review on Advanced Control Technologies for Bidirectional DC/DC Converters in DC Microgrids," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

[4] N. Swaminathan and Y. Cao, "An Overview of High-Conversion High-Voltage DC–DC Converters for Electrified Aviation Power Distribution System," in *IEEE Transactions on Transportation Electrification*, vol. 6, no. 4, pp. 1740-1754, Dec. 2020.

[5] L. Tarisciotti, A. Costabeber, L. Chen, A. Walker and M. Galea, "Current-Fed Isolated DC/DC Converter for Future Aerospace Microgrids," in *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2823-2832, May-June 2019.

[6] L. Tarisciotti, A. Costabeber, C. Linglin, A. Walker and M. Galea, "Evaluation of Isolated DC/DC Converter Topologies for Future HVDC Aerospace Microgrids," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, 2017, pp. 2238-2245.

[7] R. Chen et al., "A Cryogenically-Cooled MW Inverter for Electric Aircraft Propulsion," *2020 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS)*, New Orleans, LA, USA, 2020, pp. 1-10.

[8] R. T. Naayagi, "Bidirectional DC-DC Converter for Aircraft Electric Energy Storage Systems," Ph.D. dissertation, Sch. Elect. and Electron. Eng., Univ. Manchester, Manchester, UK, 2010.

[9] Y. Du, E. Aeloiza and V. R. V. Ramanan, "A High Current Bidirectional DC-DC Converter for Concept Demonstration of Grid-scale SMES Systems," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, USA, 2016, pp. 1-8.

[10] Q. Sun et al., "Design and Test of a New Two-Stage Control Scheme for SMES-Battery Hybrid Energy Storage Systems for Microgrid Applications", *Applied Energy*, vol. 253, p. 113529, 2019.

[11] H. Alafnan et al., "Application of SMES-FCL in Electric Aircraft for Stability Improvement," in *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 5, pp. 1-6, Aug. 2019, Art no. 5000906.

[12] J. Jin, X. Chen, X. Zhou, W. Xu, Y. Zhang and Y. Xin, "Development of a New Bridge-type Chopper for Low-voltage SMES Applications," *2013 IEEE Energy Conversion Congress and Exposition*, Denver, CO, USA, 2013, pp. 5258-5265.

[13] D. Segaran, "Dynamic Modelling and Control of Dual Active Bridge Bi-directional DC-DC Converters for Smart Grid Applications," Ph.D. dissertation, Dept. Elect. and Comput. Eng., Monash Univ., Melbourne, Australia, 2006.

[14] S. Shao, H. Chen, X. Wu, J. Zhang and K. Sheng, "Circulating Current and ZVS-on of a Dual Active Bridge DC-DC Converter: A Review," in *IEEE Access*, vol. 7, pp. 50561-50572, 2019.